ABSTRACT OF THE DISCLOSURE

In a dynamic circuit, when only between a precharge node and an intermediate node through a plurality of logical-operating MOS transistors is conducted, the potential of the precharge node approximately drops to High*{C1/(C1 + C2)} from High, where C1 represents the capacitance of the precharge node and C2 represents the capacitance of the intermediate node. Thereafter, with the charge from a power supply, the precharge node returns to High. At this charge sharing time, the amount of charge supply from the power supply is adjusted to suppress voltage drop of the precharge node, thereby reducing noise.